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PATENT APPLICATION FOR

METHOD FOR FABRICATING A MICROELECTROMECHANICAL SYSTEM (MEMS) DEVICE USING A PRE-PATTERNED SUBSTRATE

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CROSS-REFERENCE TO RELATED APPLICATIONS

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BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to microelectromechanical systems (MEMS) and, in particular, relates to the fabrication of MEMS structures.

2. Discussion of the Related Art

[0002] Microelectromechanical Systems (MEMS) components are being progressively introduced into many electronic circuit applications and a variety of micro-sensor applications. Examples of MEMS components are electromechanical motors, radio frequency (RF) switches, high Q capacitors, pressure transducers and accelerometers. In one application, the MEMS structure is an accelerometer having a movable component that, in response to acceleration, is actuated so as to vary the size of a capacitive gap. Accordingly, the electrical output of the MEMS structure provides an indication of the strength of the external stimulus.

[0003] One method of fabricating such components, often referred to as surface micro-machining, uses a sacrificial layer, such as silicon dioxide, that is deposited and bonded onto a substrate, such as single crystal silicon which has been covered with a layer of silicon nitride. A MEMS component material, for example polycrystalline silicon, is then deposited on the sacrificial layer, followed by a suitable conductor, such as aluminum, to form an electrical contact with the ambient environment. The silicon layer is then patterned by standard photolithographic techniques and then etched by a suitable reactive ion etching plasma or by wet chemistry to define the MEMS structure and to expose the sacrificial silicon dioxide layer. The sacrificial layer is then etched to release the MEMS component.

[0004] Several disadvantages are associated with fabricating a MEMS structure using a sacrificial layer. First, it requires an etching process that selectively etches the sacrificial layer without reacting with the other materials that will ultimately form the MEMS structure. This limits the materials that may be used when fabricating the MEMS structure. Additionally, the use of a sacrificial layer increases the amount of materials needed to form the MEMS structure, thereby adding cost to the fabrication process. Furthermore, an additional etching step is needed to remove the sacrificial layer, thereby further reducing the efficiency of the fabrication process. In particular, because the structure forming the movable MEMS element is disposed above the sacrificial layer, a significant amount of time is needed to completely undercut the sacrificial layer.

[0005] What is therefore needed is an improved method for fabricating a MEMS structure that avoids the inefficiencies associated with the use of a sacrificial layer.

BRIEF SUMMARY OF THE INVENTION

[0006] The present inventors have recognized that a recess may be pre-etched in a substrate for a MEMS structure that facilitates release of the device.

[0007] In accordance with an aspect of the invention, a method of fabricating a MEMS structure includes attaching an etchable wafer to an upper surface of a substrate having a recess formed therein. The wafer includes a wafer portion from which a movable MEMS structure will be formed. The wafer is attached onto the substrate so that the wafer portion is positioned above the recess. Next, the wafer is etched downwards around the periphery of the movable structure to break through into the recess to release at least part of the movable structure from the substrate. This method therefore foregoes the need to perform substantial undercutting of a sacrificial layer.

[0008] The above aspects of the invention are not intended to define the scope of the invention for which purpose claims are provided. In the following description, reference is made to the accompanying drawings, which form a part hereof, and in which there is shown by way of illustration, and not limitation, a preferred embodiment of the invention. Such embodiment does not define the scope of the invention and reference must be made therefore to the claims for this purpose.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Reference is hereby made to the following figures in which like reference numerals correspond to like elements throughout, and in which:

[0010] Fig. 1 is a schematic sectional side elevation view of an SOI wafer and a substrate that will form a composite structure in accordance with the preferred embodiment;

[0011] Fig. 2 is a sectional side elevation view of the substrate as illustrated in Fig. 1 after performing a standard photolithographic patterning process and an etching procedure;

[0012] Fig. 3 is a sectional side elevation view of the wafer illustrated in Fig. 1 bonded to the substrate illustrated in Fig. 2 to form a composite structure;

[0013] Fig. 4 is a sectional side elevation view of the composite structure illustrated in Fig. 3 having a portion of the SOI wafer removed and additional layers deposited in accordance with the preferred embodiment;

[0014] Fig. 5 is a sectional side elevation view of the composite structure illustrated in Fig. 4 having photoresist applied to the upper surface thereof;

[0015] Fig. 6 is a sectional side elevation view of the composite structure illustrated in Fig. 5 following photolithographic patterning and etching of the topmost layer and photoresist removal;

[0016] Fig. 7 is a sectional side elevation view of the structure illustrated in Fig. 6 after etching a conductive layer of the wafer;

[0017] Fig. 8 is sectional side elevation view of the structure illustrated in Fig. 7 after further etching the wafer;

[0018] Fig. 9 is a schematic sectional side elevation view of the fabricated structure illustrated in Fig. 8 after further photolithographic patterning and etching of the wafer; and

[0019] Fig. 10 is a schematic sectional side elevation view of a fabricated MEMS structure constructed in accordance with an alternate embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] Referring initially to Fig. 1, the components of a MEMS structure include a silicon-on-insulator (SOI) wafer 20 and a substrate 22 (which could be either non-conductive or conductive). The wafer 20 includes an upper and lower layer of silicon 26 and 28, respectively, that are separated by a first layer of nonconductive silicon dioxide 24. As will become more apparent from the description below, the thickness of layer 28

will ultimately define the thickness of the resulting MEMS structure. It should be appreciated that SOI wafers are commercially available having thicknesses for layer 28 of between 1 and 100 microns. The thickness of layer 26 may vary between, for example, 350 and 750 microns, and can depend on the diameter of the wafer. Such SOI wafers are commercially available, for example, from Shin-Etsu Handotai Co., Ltd., located in Japan.

[0021] A second layer of silicon dioxide 30 is grown or deposited on the lower surface 29 of the silicon layer 28, for example by using a plasma enhanced chemical vapor deposition process (PECVD) as is understood by those having ordinary skill in the art. Alternatively, layer 30 could comprise silicon nitride. The silicon dioxide layer is added in accordance with the preferred embodiment to facilitate a mechanical connection, that is electrically isolating, between different portions of the MEMS structure. It should be appreciated, however, that the substrate 22 may be either conducting or nonconducting, and may therefore alternatively comprise high resistivity silicon, crystalline sapphire, crystalline silicon, or poly-crystalline silicon, silicon carbide, or a ceramic such as alumina, aluminum nitrite, and the like, or gallium arsenide. Accordingly, the substrate may be conducting or nonconducting, depending on the fabricated MEMS structure and its application. It may be desirable to employ a silicon substrate when producing a silicon MEMS structure to ensure that the thermal and mechanical properties of the substrate and MEMS structure match to make processing easier and to eliminate the possibility of undesirable thermally induced stresses. On the other hand, it may be desirable to employ non-conducting substrates when very high electrical isolation is necessary.

[0022] Referring now to Fig. 2, a recess 32 is formed in the upper surface 23 of the substrate 22 by placing photoresist on the substrate and patterning it with standard photolithographic techniques such that, when etched, the portion of the substrate having the photoresist remaining thereon will remain intact, while the exposed material will be removed. Accordingly, to form the recess 32 in the middle portion of the upper surface 23 of the substrate 22, the photoresist is patterned to remain on the outer portions of the upper surface, and the substrate 22 is etched using a plasma etch or wet chemistry etch suitable for the material composition of the substrate, as is understood by those having ordinary skill in the art. It should be appreciated that several MEMS structures may be fabricated from a single wafer, and that photoresist in such embodiments is patterned in accordance with the present invention by providing gaps therebetween, wherein the gaps will ultimately define the recesses 32 in the wafer.

[0023] The photoresist is removed to reveal the recess 32 having beveled side walls 33. While the recess 32 is shown as being isotropically etched in the figures, thereby producing the beveled walls 33, it should be appreciated that an anisotropic etching process (for example, using an anisotropic etching plasma) could alternatively be used, which would produce side walls that are substantially perpendicular to the upper surface of the substrate 22. The recess 32 is chosen to be sufficiently deep so as to enable the MEMS structure to release from the substrate 22 after fabrication, as will be described in more detail below.

[0024] While the recess 32 has been described in accordance with the preferred embodiment, other methods of releasing the substrate could be implemented as described in patent application entitled "Method for Fabricating an Isolated Micro-Electromechanical System Device Using an Internal Void" filed on even date herewith, the disclosure of which is hereby incorporated by reference as if set forth in its entirety herein.

[0025] Referring now to Fig. 3, the bottom surface 31 of the silicon dioxide layer 30 is bonded to the upper surface 23 of the substrate 22. In particular, the wafer 20 is positioned above the insulating substrate 22, and is bonded thereto via, for example, high temperature fusion bonding or any other suitable process as understood by those having ordinary skill in the art. Because the wafer 20 does not need to be bonded to the substrate 22 using a layer that will need to be undercut in a subsequent procedure, as in prior art fabrication methods, the bond will not be sensitive to temperature elevations that may occur at later stages of the fabrication process. It should be appreciated that, depending on the material chosen for the substrate 22, it may be desirable to grow or deposit an oxide layer onto the upper surface 23 thereof prior to the bonding step in order to provide a suitable layer to bond with the lower surface 31 of the silicon dioxide layer 30.

[0026] Referring also now to Fig. 4, the relatively thick silicon base layer 26 is mostly removed by a grinding and polishing process, and is finished by subsequently etching in tetramethylammonium hydroxide (TMAH) to expose silicon dioxide layer 24. In this regard, layer 24 provides an easily controlled etch stop when removing layer 26 as it is not etched by TMAH. The oxide layer 24 is then removed by etching with hydrofluoric acid to reveal an upper surface 27 of the silicon layer 28. The layer 28 remains having the desired uniform thickness, it being appreciated that the final height h of the wafer 20 will correspond generally to the desired height of the resulting fabricated MEMS structure, as will become more apparent from the description below.

[0027] The same desired structure can also be obtained without the use of an SOI wafer, but with a simple silicon wafer instead. Accordingly, the wafer 20 could comprise silicon, silicon carbide, or gallium arsenide. If the wafer 20 is not an SOI wafer, it would be ground and polished to the desired thickness after bonding. The use of commercially available SOI wafers facilitates the attainment of the desired silicon thickness. Also, additional silicon from layer 28 may be removed from the SOI wafer 20, if so desired, by grinding and polishing.

[0028] Next, a conductive layer 36, such as aluminum, is deposited onto the upper surface 27 either by evaporation or sputtering, or any suitable alternative process, as is well known in the art. The conductive aluminum layer 36 will eventually form the electrical contact for the MEMS structure after the fabrication process has been completed, as will become more apparent from the description below. Alternative suitable conductors may be deposited besides aluminum, such as copper, silver, gold or nickel, or a highly doped semiconductor material such as silicon, silicon carbide, and gallium arsenide, or any other suitable conductive metal that is compatible with the fabrication processes of the present invention. Next, a silicon dioxide layer 38 is deposited onto the upper surface 37 of the aluminum layer 36 to provide protection for the aluminum layer 36 and to provide a mask for future etching of the aluminum and silicon. Alternatively, the layer 38 could comprise silicon nitride. Specifically, the layer 38 may be deposited using the aforementioned PECVD process, or other well known methods. Alternatively, photoresist could be used instead of layer 38 to provide a pattern for etching through both the aluminum and silicon layers 36 and 28. Because layer 38 is subsequently removed regardless during a subsequent fabrication process, as will be described in more detail below, the resulting MEMS structure 58 has the composition whether or not layer 38 is used as a protective layer.

[0029] Once the desired layers are in place, they are etched so as to form the MEMS structure in accordance with the preferred embodiment. Referring in particular to Fig. 5, the etching process of the wafer 20 begins by depositing a photoresist layer and patterning by standard photolithographic techniques to leave inner and outer members 42 and 44, respectively, having a gap 41 disposed therebetween that is at least partially aligned with recess 32. As will become more apparent from the description below, gap 41 will become a variable size gap separating a movable MEMS element 52 from a stationary MEMS element 50 (shown in Fig. 9) once the wafer 20 has been completely etched. The recess 32 is disposed in the substrate 22 so as to allow the fabricated movable MEMS

element to be released from the substrate upon etching. Accordingly, the wafer 20 is etched into the recess 32, thereby releasing the movable MEMS element, as will be described in more detail below. Advantageously, the movable MEMS element will accordingly be released without the need to undercut a sacrificial layer. It should be appreciated that Fig. 5 is a schematic illustration whose purpose is to illustrate the conceptual placement of the photoresist in relation to the recess 32, and could assume any configuration whatsoever that would produce a suitable MEMS structure and facilitate the release of the movable MEMS element.

[0030] Referring now also to Fig. 6, the upper surface 39 of the silicon dioxide layer 38 is patterned by standard photolithography techniques to produce a structure which will define the stationary and movable MEMS elements 52 and 50 (shown in Fig. 9), respectively. In accordance with the preferred embodiment, the silicon dioxide layer 38 is etched, for example, by using a dry anisotropic etching plasma, such as trifluoro-methane (CHF_3), commercially known as fluoroform. The etching continues until all silicon dioxide disposed between photoresist members 42 and 44 has been etched, thereby exposing the conductive aluminum layer 36. The photoresist is removed using the appropriate solvent for the photoresist material used. Because the etched silicon dioxide layer 38 is selectively etchable from the remaining materials that comprise wafer 20, layer 38 will therefore provide the structure necessary to define the etching pattern for subsequent etching processes, as will now be described. As described above, if layer 38 is not present, the photoresist will provide the structure necessary to define the subsequent etching processes.

[0031] Referring to Fig. 7, the aluminum layer 36 is etched, for example, by using an anisotropic etching plasma that selectively etches aluminum, and that does not react to either silicon dioxide or silicon. A chlorine plasma has been found to be suitable for anisotropically dry etching the aluminum layer 36 in accordance with the preferred embodiment. Because the plasma does not react with silicon dioxide or silicon, the resulting etched aluminum structures 36 are vertically aligned with the previously etched silicon dioxide layer 38. Once the aluminum has been etched, the silicon layer 28 is exposed and ready to be etched as will now be described with reference to Fig. 8.

[0032] Specifically, the silicon layer 28 is anisotropically dry etched by a process commonly referred to as Deep Reactive Ion Etching (DRIE), which involves setting up a reactive etching environment in a suitably chosen gas by exciting with an inductively coupled plasma (ICP), as is understood by those having ordinary skill in the art. Because

silicon dioxide is not etched under the same conditions as silicon, the silicon layer 28 is etched until the silicon dioxide etch stop layer 30 is revealed to produce a pair of stationary outer structures 50 and an inner set of structures 52 that will ultimately define a stationary conductive MEMS element and a movable MEMS element, respectively, as will be described in more detail below.

[0033] Next, referring to Fig. 9, the silicon dioxide layers 30 and 38 are photolithographically patterned and anisotropically etched, for example, in fluoroform, in accordance with the preferred embodiment, though it should be easily appreciated that any suitable etchant may be used. Layers 36 and 28 as well as patterned photoresist aligned with the inner MEMS element 52 (not shown), provide the structure necessary to define the etching pattern for the etching of layer 30, such that only that silicon dioxide in layer 30 that is aligned with gap 41 is removed. It should be appreciated that the silicon dioxide in layer 30 that is aligned with the gap connects the inner structure 52 to the outer structures 50. Accordingly, etching this silicon dioxide creates stationary outer MEMS elements 50 and additionally releases the movable MEMS element 52 from the substrate 22 without the need to deposit and subsequently undercut a sacrificial layer, as in prior art fabrication techniques. As a result, only those materials that ultimately form the fabricated MEMS structure 58 are used in the fabrication process. The release of the movable MEMS element 52 additionally transforms gap 41 into a variable size gap 41, whose size may be used to define the capacitance of the MEMS structure, as will be described in more detail below.

[0034] While layer 38 is removed in accordance with the preferred embodiment, layer 38 could remain as part of the fabricated MEMS structure 58 to provide a protective layer for the aluminum layer 36.

[0035] The final MEMS structure 58 therefore includes stationary outer MEMS elements 50, and an inner movable MEMS element 52. It should be appreciated, however, that wafer 20 could alternatively be etched in accordance with the present invention to produce any MEMS structure having a suitable configuration that facilitates the release of a movable MEMS element. The outer and inner MEMS elements 50 and 52 include a silicon layer 28 separated from the substrate 22 by a non-conductive layer of silicon dioxide 30, thereby providing electrical isolation on the order of 2000 volts. A conductive layer of aluminum 36 is disposed above the silicon layer. In accordance with the preferred embodiment, a wire may be connected to the aluminum layers 36 of the

stationary MEMS elements 53 to place the stationary elements in electrical communication with the ambient environment and render the device 58 operable.

[0036] The preferred embodiment of the invention could thus be implemented to form a MEMS structure incorporating a wafer level cap, having electrical leads extending from the base of conductive elements 50 to the ambient environment outside the cap, as described in a patent application entitled «Method for Fabricating an Isolated Microelectromechanical System (MEMS) Device Incorporating a Wafer Level Cap" filed on even date herewith, the disclosure of which is hereby incorporated by reference as if set forth in its entirety herein.

[0037] Referring now to Fig. 10, the MEMS structure 58 is illustrated in accordance with an alternate embodiment of the invention, wherein the SiO_2 layer 30 has been replaced with a silicon base 45. In order to provide electrical isolation between the inner MEMS structure 52 and outer conductive elements 50, a layer of silicon dioxide 43 is disposed between the silicon 28 and aluminum 36 on the outermost inner MEMS finger disposed proximal the interface between field and control sides of the integrated circuit, as an example. Layer 43 is sufficient to provide low level electrical isolation on the order of 50 volts, suitable for typical integrated circuits. Accordingly, this embodiment is desirable when the fabricated MEMS structure 58 does not require the 2000 volt isolation achieved by oxide layer 30. Furthermore, this embodiment is easier to fabricate and is stronger due to the uniformity of materials used to fabricate inner element 52.

[0038] The MEMS structure 58 could therefore perform any function suitable for a MEMS application. For example, the device 58 could comprise an accelerometer whose movable MEMS element 52 is a cantilever beam that deflects in response to an external stimulus, such as an acceleration or vibration of the device 58. Accordingly, as the size of the gap between the stationary conductive elements 50 and the movable MEMS element 52 varies, so will the output capacitance, thereby providing a measurement of the amount of deflection of the movable MEMS element 52. A measurement of the strength of an external stimulus may thereby be obtained.

[0039] It should be appreciated by one having ordinary skill in the art that a portion of a MEMS structure 58 has been illustrated, it being appreciated that inner MEMS element 52 is connected to substrate 22 at its two distal ends, as described in patent application filed on March 13, 2001 and entitled "Microelectricalmechanical System (MEMS) Electrical Isolator with Reduced Sensitivity to Internal Noise» the disclosure of which is hereby incorporated by reference. For example, the void 32 that is disposed in substrate

22 may terminate, thereby connecting element 52 to the substrate. In accordance with the preferred embodiment, an elongated section of element 52 is suspended and free from the substrate, thereby permitting deflection of the free portion of the movable MEMS element with respect to the substrate 22. An electrical trace may be connected to the movable element 52 at these connection locations.

[0040] The above has been described as a preferred embodiment of the present invention. It will occur to those that practice the art that many modifications may be made without departing from the spirit and scope of the invention. For example, while the various layers are described as being made of silicon, silicon dioxide, and aluminum, any other suitable compositions could be used that have the desired conductive or insulating properties. In order to apprise the public of the various embodiments that may fall within the scope of the invention, the following claims are made.